Skills and Accomplishments Packet

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Waferfab

Diffusions: Sources: Vapor ($POCl_3$, B_2H_6, PH_3), solid source (BN, disk B_2O_3, disk P_2O_5, etc.), spin-on and paper diffusions of epitaxial and double diffused power zeners, rectifiers and transistors from 6.2 through 1600 volt (single junction) and over 10,000 volt (multi-junction). Contracted some ion implant work.

Spin-On: Developed and patented an in-house spin-on dopant system allowing simultaneous P+ and N+ high Css diffusions up to 200 µM. System allowed drives in stand-up ladder boats without wafer sticking, cross contamination or wafer warping. Dopants were patented.
Developed technique for selective etch and thermal oxidation masking using silicon nitride.

Alloy Junction: Had full product and process responsibilities for production, targeting and special handling of the TRW LVA zener. Produced many aluminum alloy junctions including micro junction low voltage and standard zeners.

Lifetime Control: Formulated in-house spin-on lifetime control dopants such as gold and platinum. Pioneered platinum doping of high-speed double slug glass rectifiers from 100 volt to 1600 volt. Product is still in production. Extensive computer modeling was employed.

Platinum Bipolar: Developed first platinum enhanced Bipolar switching power transistor. Technique allowed direct competition with power MOS-FETs of the time with superior current handling and higher voltage capability (10 Amp 900 volt).

Gettering: Implemented low stress diffusion schemes using ramp up and down programming along with TCA (1-1-1 Trichloroethane) injection for metal gettering and lattice annealing. Higher transistor gains and superior high current roll-off characteristics plus flatter lower current gain resulted. Employed TCA to purify alkali and heavy metal contaminated diffusion furnaces on a regular basis. When possible, tied C-V (capacitance-voltage) SPC monitoring to these purification cycles.

Thin Film: Deposition: Experienced with multi-hearth E-Beam and filament evaporation of titanium, aluminum, gold, nickel and silver.

Barrier: Associated with sputtered Schottky Barrier film processes such as nichrome, nichrome-platinum, tungsten silicide and platinum silicide. Wrote very detailed Schottky Barrier emulation models called SECal.

CVD: Vapor deposition of SiO_2 and Si_3N_4 using silane and silicon tetrachloride with various reactive gasses such as O_2, NH_3 and HCl. Developed non-polluting ecologically safe phosphoro-silicate and boro-silicate CVD film techniques using non-toxic unpressurized liquid sources.

Nitride: Associated with low temperature plasma nitride etch/deposition (Tegal 302) for over-metal passivation of 800 volt Darlington power transistor.

Glassivation: Developed and introduced numerous low and high temperature glassivation processes for zener and rectifier products to 1600 volts using doctor blade, photo glass and centrifuge deposition techniques.

Thermal Oxides: Experienced with thermal oxidation of silicon including dry, "damp", and wet (bubbler, steam, hydrogen torch, TCA enhanced, etc.) as well as etching and masking properties. I have written programs to model oxide growth and dopant masking.

Sputtered Insulators: A major project was the study of sputtered SiO_2 and Si_3N_4 films for junction passivation of rectifiers up to 2000 volt Es. The study included cause and effect of free charges, both polar and ionic, and led to techniques for the reduction of these elements. Metallic ion mobility and trapping were also considered. This project resulted in the pioneering of a specially modified diode annular ring sputtering system that I then put into production depositing these films.

Photo: Aligners: Familiar with aligners and aligner light-optics systems. Introduced light intensity and light uniformity monitoring equipment and procedures. Have even repaired aligners when necessary.

Masks: Have designed and implemented multi-layer transistor, SCR, zener and rectifier photomasks. I can complete a CAD mask design in DWG format and wire it directly to mask maker for direct conversion into photomask plates.

Resists: Experienced with Hunt negative resists over a wide viscosity range (900 to 43). Have done some work with Shipley positive resists as that is the resist of choice for Schottkys.

Assembly

Packaging: Glass: Glass voidless monolithic double slug bonded die A, B, C and MELF package structures.

Metal: Metal packages such as TO-3, DO-4 and 5, TO-59(I), TO-61(I), TO-18, DO-13, etc.

Flat: Flat packages such as TO-257, TO-254, TO-258, TO-259, TO-267, SIP's and DIP's (with/without substrates of alumina or berylia, thick film or DBC).

Surface: SMD (Surface Mount Device) packages such as SMD-1, SMD-2, LCC, SMD ribbon leaded, etc. in alumina, berylia and aluminum nitride employing seam welded and brazed lids.

Bond: Wire bond using aluminum (1 to 20 mil) and gold (0.8 to 3 mil). Have modeled wire DC and transient power capability to establish design rules for production. Models were placed under document control system.

Molded: Epoxy transfer molded commercial packages (axial, TO-218, etc.) including lead frame die bonding and lead plating.

Filled: Special assembly epoxy filled high voltage and high power devices including stacks, high-energy transient voltage suppressors, rectifier bridges, voltage multipliers and other custom designs.

Metallurgy: Brazing: Set up low and medium temperature lead-to-slug brazing of copper, silver, nickel and dumet wires to nickel and silver plated moly and tungsten slugs.

Solder Dip: Experienced with manual and automatic solder dipping of all manner of axial and power packages as well as use of both commercial and my own developed fluxes.

Soft Braze: Replaced gold-silicon hand scrubbed die mount with some of the earliest implementation of PbInAg clad moly and copper tabs thereby eliminating all precious metal usage. Familiar with capping environment and materials issues that lead to premature IOL (Intermittent Operating Life) failures.

Copper Bond: Studied and modeled material dynamics necessary to mount silicon (up to 375 x 375 mils) directly onto copper for cost reduction without sacrificing reliability in power supply applications. I am very familiar with lead-tin and lead-indium-silver die attach techniques.

Plating: Tin-Lead Plate: Introduced methane-sulfonic acid barrel tin plating and, later, tin 5% lead plating process into production with effective pre-cleaning. Designed plating barrels and developed computer models to enable production to plate a wide variety of product types and quantities. These models were flexible and accurate and could automatically generate the barrel loading tables that appeared in the appendix of the plating procedure.

Electroless: Developed several electroless nickel-over-silicon plating processes employing boron and phosphorous nickels. Specially developed activators permitted plating over heavily doped P+ and N+ silicon overcoming galvanic polarization of P+ and N+ in the plating solution. Designed a complete silicon wafer electroless nickel plating process starting with cost effective computer designs of all the equipment up through all of the chemistry, controllers, automatic and manual bath chemical analysis procedures. A low-cyanide gold finishing plating process was also included for the project. Designed and set-up boron-nickel barrel pulse plating of molybdenum for use in a low cost glass diode which I developed.

Silver Contact: Developed and put into production heavy silver plate-through-mask metallization for Schottky rectifier wafers. Used a coiled wafer fixture that permitted rapid loading and unloading of large quantities of wafers. Also set up selective silver bump plating of computer diode and micro junction zener wafers.

Silver Bump: Introduced process to plate silver bumps on computer diodes, signal Schottky diodes and 1A military glass sealed Schottkys. Developed plating model that allows anyone to design any kind of bump with any kind of metal on any kind of wafer.

Immersion: Created numerous immersion and electroless plating systems for copper, tin, gold, silver, gold-tin alloys, nickel-palladium and others.

Test

Equipment: Lifetime: T_{rr} testing: Designed and built special t_{rr}, t_r and t_f test gear with 2 Amp per nanosecond slew rates and up to 5 ampere capability. Most theoretically perfect pulse switching waveform in the industry both then and now.

Thermal Impedance: Designed and built thermal impedance testers and modeled device transient response. Designed system to measure zone thermal impedance of die-to-header contact within milliseconds, long before commercial equipment such as the Sage and Farratron was available. I am very familiar with the FEC thermal impedance test system, the current standard in the industry. I have made formal presentations to JC-13 and G-12 on thermal impedance techniques and principles.

Surge Test: One of the pioneers in the use of power surge testing for reliability screening. Designed and built own equipment. Later used FEC VF-40, PLS-600, 800 and PLS-1000 equipment for most recent work (surge and thermal impedance; fully automated).

Die Testing: Set-up automatic dice testing using vacuum 4-point probe system for diodes up to several amperes and up to 600 volts. Also associated with test procedures and techniques for testing Bipolar power transistor die. Worked with wafer probers.

Automatic: Worked with, programmed and optimized FEC automatic component testers.

QA/QC

Reliability: Documentation: Wrote process documents and worked such programs as Minuteman, Apollo, Thor-Delta, Saturn, etc. Also had full engineering and marketing responsibilities on ARM, Redeye and Standard Missile at General Dynamics.

Simulation: Developed computer models to simulate power burn-in requirements on a variety of equipment including Microinstruments and E-J Systems plus conventional resistor ballested burn-in gear. I then converted this into detailed, self-correcting instruction tables for QA to easily follow. I wrote a burn-in and HTRB model to prevent thermal runaway.

Failure Analysis: Studied and developed techniques for cross-sectioning, special decorative junction staining and various metallurgical stains. Conducted numerous failure analyses. Worked with low and high energy X-Ray for void detection.

Lattice Distortion: Studied silicon crystal dislocation cause-and-effect. Special preferential etches were employed. Developed process techniques to eliminate or control damage site generation, metal impurity migration and chronic wafer breakage problems.

IOL: Studied failure mechanisms in IOL (Intermittent Operating Life) and changed or influenced the change of braze alloy specifications, vendors, package sealing/capping environment, furnace profiles, furnace leak integrity, etc. Addressed a major problem of trapped hydrogen virtual water leaks with a strategy to minimize its influence past 6000 cycles.

SPC: Easily the biggest challenge a semiconductor manufacturer can face----I have received SPC (Statistical Process Control) training both in-house at Semicon and at Hamilton Standard in their vendor training programs. I want to implement SPC where it will do the most good and to recognize where it won't. I created computer templates for all the SPC chart requirements.

Government—Industry

JC-13: Have been a member of EIA (Electronic Industry Association) JC-13.1 over 25+ years with active participation on various committees covering a wide technological base. I founded and was the Chair of JC-13.1 Task Group 9813 until we successfully completed our mission by updating the Mil-Std-750 die visual specifications. I also Chaired the JC13.1 Leak Rate Task Group.

DLA: I have worked with and consulted for DSCC (Defense Supply Center Columbus) later DLA (Defense Logistics Agency) and have enjoyed the relationship immensely. I've been technical consultant to JC-22 and have made technical presentations to G-12. I've received a number of awards in this role. Later I became the Chair of JC22.

Computer Modeling and Simulation

Models: Schottkys and Rectifiers: Modeled PN and Schottky rectifiers to predict forward and reverse characteristics under a wide variation of temperature, doping and lifetime conditions. Both vertical and horizontal geometries were included.

Small Signal and Power Transistors: Modeled power and small signal switching transistors to accurately predict reverse and conduction parameters using simulated two and three-dimensional analysis. Guard rings, peak gain, C-V profiles, high current roll off, sustaining voltage and storage

time (saturated and non-saturated) were included. These models were designed and made available to general engineering staff.

Thermal Analysis: Wrote thermal transient heat flow analysis software for multi-layered semiconductor structures. These models included both analog and finite element models capable of analyzing a wide variety of static and transient power stress conditions. In this area I have been a technical resource for DESC (Defense Electronic Supply Center, later DLA) as well as for several industry colleagues.

Ion Implant: Modeled ion implant profiles for transistor base depositions with treatment of annealing and re-distribution diffusions.

Finite Element: Current plan is to interface Excel to Stanford University's public domain SUPREM and PISCES (the basis of Silvaco's very expensive semiconductor models) so that every engineer could become a wafer fabrication expert with their very own copy of the simulation software. Come to think of it, even I want a copy of this powerful tool.

Empowerment to Production: Produced translated computer models that take finite element structures analyzed with the very complex models mentioned above and translated them into fast, easy-to-use Excel VisualBASIC models suitable to predict reverse voltage and capacitance characteristics as well as forward conduction over wide temperature and lifetime conditions. These translated models were documented for permanent record in document control and the training of production/engineering in model use was made available.

Software: Proficient in Excel, Word, Project, Canvas, Filemaker, Inspiration, DenebaCAD, DeltaGraph, plus the server driven production control MAX and document control Keyfile applications. Programming experience includes QuickBASIC, VisualBASIC and some C++. Very comfortable with Windows XP/Win 7, 8 and 10 as well as Macintosh OS, OSX and of course, iOS.

General: I use the computer to the fullest. I have produced extensive technical graphic presentations on the computer for customer presentations, staff meetings and theoretical simulations. Many processes were developed directly from these models. I have done extensive device modeling. I am a perfectionist in this area, developing models which are accurate enough that new ideas can all be "computer built and tested" before ever seeing a single step of processing. This includes diode, zener and transistor diffusion, targeting and performance emulation models.

New Product-Marketing-Applications

New Product: Foundry Harvesting: Creative designs using foundry supplied Voltage Regulators, MOSFET's, IGBT's, Op-amps, Schottkys, FRED's—coupled with a multitude of package options—provides an almost inexhaustible source of new product to offer. Linear Voltage Regulators (discrete or hybrid, with or without thin film resistor trimming, surface mount capacitors or output stages) were especially successful.

New Market: Radiation Tolerant: This is a relatively new rewarding business opportunity. I understand the steps and the radiation science necessary to introduce a line of radiation tolerant components suitable for a substantial portion of orbital space applications. I created a spec sheet graphics engine that takes the radiation data and converts it directly into the appropriate spec sheet curves. A broad base of product was tested (gamma Cobalt 60 and neutron fluence) and I evaluated both to in-house specifications as well as to Mil-Prf-38534-5/Mil-Std-883 and Mil-Prf-19500/Mil-Std-750 requirements. The market "revolution" is changing from over-priced Radiation Hard components to a cost effective and wider selection Radiation Tolerant component mix.

Applications: I have traveled extensively, wearing both sales and engineering hats representing our product lines to many customers. My product, engineering, reliability and electronics background makes this area of work come naturally. I get along well with all levels at any customer: Engineering, components, project, production, QC, purchasing and senior management. I can assist the customer in application engineering problem solving, design challenges, thermal conduction considerations, package stress analysis and extreme environment assessment. I have also served as a product Sales Manager covering both the United States and Canada as part of a special project to assist a company in a time of need.

Teaching and Dissemination of Technology

Teaching: I strongly believe that no problem is ever truly solved until one can leave behind others that have been trained to take over the discipline that caused the problem in the first time. I do not believe that textbook and verbal training is sufficient and strongly support empowering the individual with easy-to-use Excel simulation models and tools that represent everything they need to know for design, targeting and support. The following few-of-many models serve as an example:
a) **LeakRate**: Allows precise control of either Helium or Radiflo leak testing with accurate directions for process control. Included the entire inventory of packages in use. Demonstrated at JC13.1.
b) **Oxide**: Provides precise targeting of any thermal oxide growth on silicon (bare or pre-oxidized) plus enables determination of doping masking time (or breeching time) and temperature.
c) **ZDDCal**: Accurate targeting of 2D (double diffused) Zener wafers with built-in reverse clamp voltage prediction using a pop-up menu of dopant processes plus select-ability of temperature and time solving both directions. Even included provisions for an active log that compared actual diffusion history while automatically providing the model predictions. Years of lots have been thus stored.

Patents

3844029 *High Power Double Slug Package*. Design permitted simultaneous silver slug end bonding with molybdenum dioxide side seals.

4039702 *Method for Settling a Glass Suspension Using Preferential Polar Adsorption*. This has become a standard in the industry for centrifugal deposition of glass.

4126713 *Forming Films on Semiconductor Surfaces with Metal-Silica Solution*. Pioneered early gold and platinum doping films.

4190458 *Metal Solution for Forming Films on Semiconductor Surfaces*. Conductive metal films palladium films on silicon.

4243427 *High Concentration Phosphoro-Silica Spin-On Dopant*. Pioneered high concentration dopant system employing alumino-phosphoro-silica spin-on dopant films.

4979076 *Hybrid Integrated Circuit Apparatus*. Design embeds chip components within the assembly board for a watertight seal or, if ceramic is used, a hermetic seal.

5113579 *Method of Manufacturing Hybrid Integrated Circuit*. Assembly process for the above design.

Pending *Room Temperature Electroless Gold Plating System*. Used to metallize devices protected with delicate glassivation systems.